REMARKS/ARGUMENTS

Claims 1-23 are pending in the present application. Claim 1 has been amended, and claim 23 has been added. No claims have been canceled. Support for the amendments to claim 1 can be found, for example, from page 21, line 17 to page 22, line 11. Applicants have carefully considered the cited art and the Examiner's comments, and believe the claims patentably distinguish over the cited art and are allowable in their present form. Reconsideration is, accordingly, respectfully requested in view of the above amendments and the following comments.

I. 35 U.S.C. § 102, Anticipation

The Examiner has finally rejected claims 1-6, 8-12, and 16-21 under 35 U.S.C. § 102(b) as being anticipated by Levine et al. (U.S. Patent No. 5,691,920). This rejection is respectfully traversed.

As to claim 1, the Examiner states:

> Referring to claim 1: Levine discloses a performance-monitoring unit (Abstract) and one or more hardware counters (column 10, lines 58-59) located within the performance monitoring unit (figure 4, structures 50 and 51). Levine discloses a variety of operations of the performance-monitoring unit (column 10, lines 34-56); Levine discloses setting the performance-monitoring unit to selectively monitor the instructions within specific addresses (column 12, 2nd paragraph). The instructions within specific addresses are a selected interrupt handling routine, and the Levine's selective monitoring on the particular instructions is the claimed hardware counters' counting the occurrence of events during an interrupt of a selected type. Furthermore, Levine discloses two separate counters for selected events (figure 6A, column 8, lines 57-60). Hence, the claim is anticipated by Levine.

Final Office Action dated March 12, 2007, pages 2-3.

Claim 1 of the present application as amended herein is as follows:

1. A data processing system for qualifying events when an interrupt occurs, comprising:
an interrupt unit control mechanism for indicating an interrupt of a selected type;
an interrupt unit, responsive to an interrupt, for determining if the interrupt is an interrupt of the selected type;
a performance monitoring unit; and
one or more hardware counters located within the performance monitoring unit;
wherein the one or more hardware counters count the occurrence of events during processing of the interrupt responsive to a determination by the interrupt unit that the interrupt is an interrupt the selected type.

Applicants respectfully submit that Levine does not identically show every element of the claimed invention arranged as they are in the claims; and, accordingly, does not anticipate the claims.

Levine is directed to a method and system for "monitoring dispatch unit efficiency in a processing system" (column 1, lines 43-45). As noted by the Examiner, Levine lists a number of performance monitoring activities that may be performed in column 10, lines 34-39. As argued previously, none of the listed activities in Levine relate to counting events occurring during processing of an interrupt; and, more particularly, none of the listed activities relate to counting the occurrence of events during processing of an interrupt of a selected type as recited in claim 1.

In order to further differentiate Levine and the present invention, and in order to expedite prosecution, claim 1 has been amended to additionally recite "an interrupt unit control mechanism for indicating an interrupt of a selected type" and "an interrupt unit, responsive to an interrupt, for determining if the interrupt is an interrupt of the selected type." In addition, claim 1 now recites that "the one or more hardware counters count the occurrence of events during processing of the interrupt responsive to a determination by the interrupt unit that the interrupt is an interrupt of the selected type." Levine nowhere discloses or suggests an interrupt unit control mechanism or an interrupt unit as now recited in claim 1, and claim 1, as amended, is not anticipated by Levine.

Claim 1, accordingly, patentably distinguishes over Levine in its present form.

Claims 2-6 depend from and further restrict claim 1, and are also not anticipated by Levine, at least by virtue of their dependency.

New claim 23 generally corresponds to claim 1 and is not anticipated by Levine for similar reasons as discussed above with respect to claim 1.

Independent claim 8 is as follows:

> 8. A method of executing instructions on an information processing system, comprising the steps of:
> receiving a signal at a microprocessor of the system for invoking an interrupt, wherein the interrupt includes a plurality of states; and
> counting at least one event for a selected state of the plurality of states during processing of the interrupt.

For similar reasons as discussed previously, Applicants continue to submit that Levine does not disclose an interrupt that includes a plurality of states, and also does not disclose "counting at least one event for a selected state of the plurality of states during processing of the interrupt".

Independent claim 16 recites similar subject matter as claim 8, and is also not anticipated by Levine for similar reasons as claim 8. Claims 9-12 and 17-21 depend from and further restrict one of claims 8 and 16 and are also not anticipated by Levine.

II. 35 U.S.C. § 103, Obviousness – Claims 1-6, 8-14, and 16-21

The Examiner has rejected claims 1-6, 8-14, and 16-21 under 35 U.S.C. § 103(a) as being unpatentable over the admitted prior art in view of Levine et al. (U.S. Patent No. 5,691,920). This rejection is respectfully traversed.

Applicants continue to submit that the Examiner has not established a *prima facie* case of obviousness with respect to the claims. As discussed in detail above, Levine does not disclose or suggest "one or more hardware counters located within the performance monitoring unit; wherein the one or more hardware counters count the occurrence of events during processing of an interrupt of a selected type" as recited in claim 1. Levine also does not disclose or suggest "an interrupt unit control mechanism for indicating an interrupt of a selected type' and "an interrupt unit, responsive to an interrupt, for determining if the interrupt is an interrupt of the selected type" as now recited in claim 1. The admitted prior art does not supply the deficiencies in Levine, and claims 1-6, 8-14 and 16-21 are, therefore, not obvious in view of the admitted prior art and Levine, and are allowable thereover in their present form.

III. 35 U.S.C. § 103, Obviousness – Claims 7, 15, and 22

The Examiner has rejected claims 7, 15, and 22 under 35 U.S.C. § 103(a) as being unpatentable over Levine et al. (U.S. Patent No. 5,691,920) in view of previously cited "Computer System Architecture" by Morris Mano or as being unpatentable over the admitted prior art in view of Levine and Mano. These rejections are respectfully traversed.

Mono is cited as disclosing monitoring interrupts according to their priority. Mono does not, however, disclose counting events separately that occur "during the processing of the interrupt of the selected type and during processing of the second interrupt" that interrupts the interrupt of the selected type as recited in claim 7. Further, Mano does not supply the deficiencies in Levine or in Levine and admitted prior art. Claim 7 and corresponding claims 15 and 22, accordingly, are allowable in their present form, and it is respectfully requested that the Examiner so find.

IV. Conclusion

For all the above reasons, it is respectfully urged that claims 1-23 are allowable in their present form, and that this application is now in condition for allowance. It is, accordingly, respectfully requested that the Examiner so find and issue a Notice of Allowance in due course.

The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

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Respectfully submitted,

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